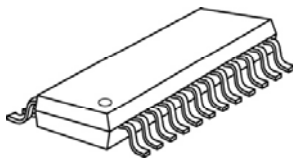
16-Channel PWM Constant Current LED Driver for 1:16 Time-Multiplexing Applications

Features

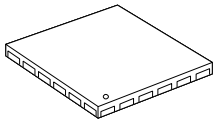
- 3V-5.5V supply voltage
- 16 constant current output channels
- Constant output current range:
  - 0.5~20mA @ 5V supply voltage
  - 0.5~10mA @ 3.3V supply voltage
- Excellent output current accuracy:
  Between channels:：<±2.5%(Max.)
  Between ICs: <±3%(Max.)
- Built-in 8K-bit SRAM to support time-multiplexing for 1 ~ 16 scans
- 14-bit /13-bit color depth PWM control to improve visual refresh rate
- 6bit current gain，12.5%~200%
- LED failure isolation
  -LED failure induced cross elimination
- LED open detection
- Integrating ghost elimination circuit
- GCLK multiplier technology
- Maximum DCLK frequency: 30MHz
- Package MSL Level: 3

Shrink SOP



GP: SSOP24L-150-0.64

Quad Flat No-leads



GFN: QFN24L-4x4-0.5

Product Description

MBI5252 is designed for LED video applications using internal Pulse Width Modulation (PWM) control with selectable 14-bit / 13-bit color depth. MBI5252 features a 16-bit shift register which converts serial input data into each pixel's gray scale of the output port. Sixteen regulated current ports are designed to provide uniform and constant current sinks for driving LEDs with a wide range of V_F variations. The output current can be preset through an external resistor. The innovative architecture with embedded SRAM is designed to support up to 1:16 time-multiplexing applications. Users only need to send the whole frame data once and to store in the embedded SRAM of the LED driver, instead of sending every time when the scan line is changed. It helps to save the data bandwidth and to achieve high grayscale with very low data clock rate. With scan-type Scrambled-PWM (S-PWM) technology, MBI5252 enhances PWM by scrambling the "on" time of each scan line into several "on" periods and sequentially drives each scan line for a short "on" period. The enhancement equivalently increases the visual refresh rate of scan-type LED displays. In addition, the innovative GCLK multiplier technique doubles visual refresh rate.

MBI5252 drives the corresponding LEDs to the brightness specified by image data. With MBI5252, all output channels can be built with 14-bit color depth (16,384 gray scales). When building a 14-bit color depth video, S-PWM technology reduces the flickers and improves the image fidelity.

Through compulsory error detection, MBI5252 detects individual LED for open-circuit errors without extra components. MBI5252 equipped an innovative cross elimination function, and it solves the cross phenomenon induced by failure LEDs. Besides, integrated ghost elimination circuit eases the ghost problems.

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Block Diagram

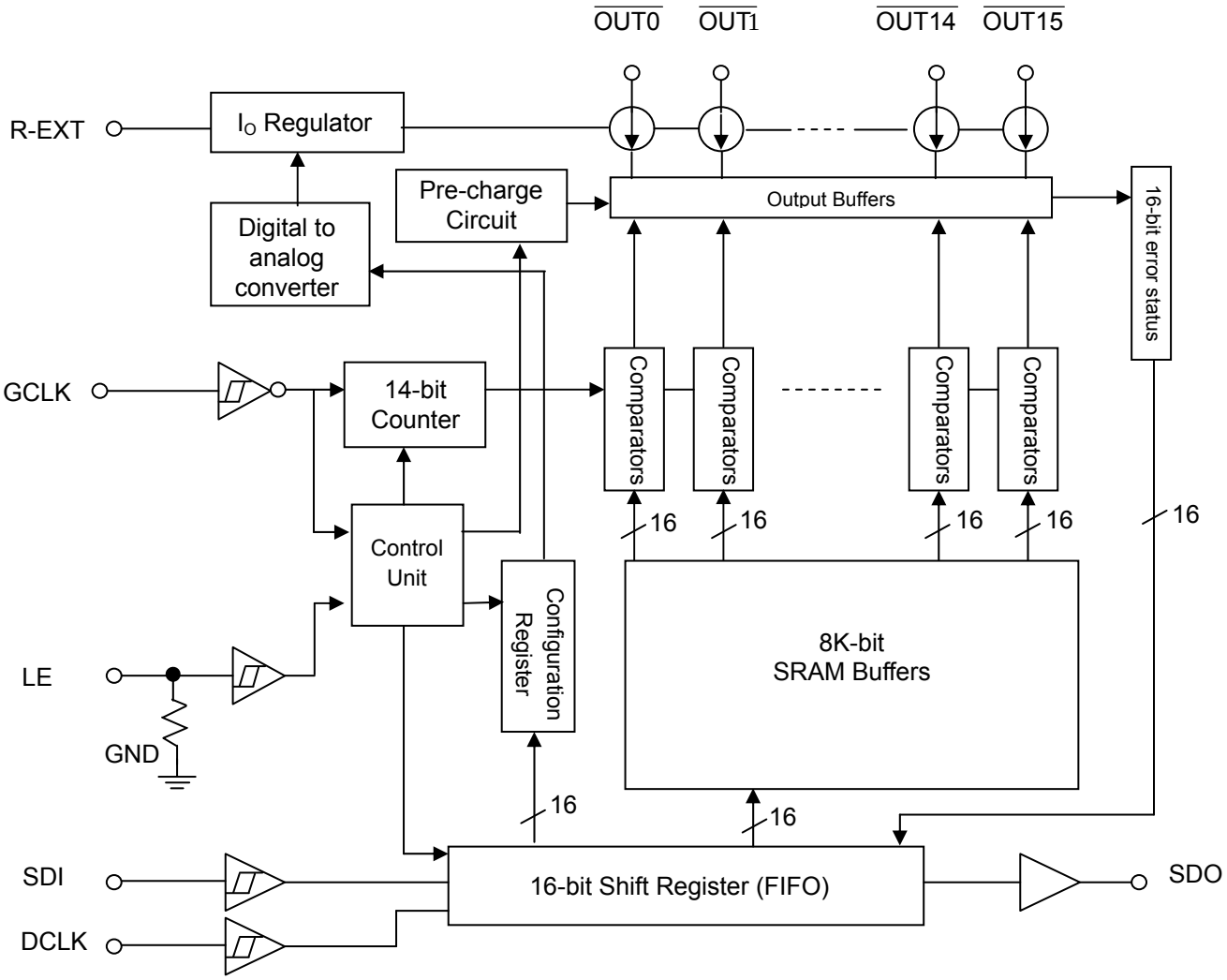
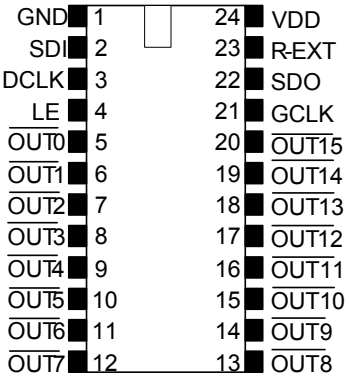
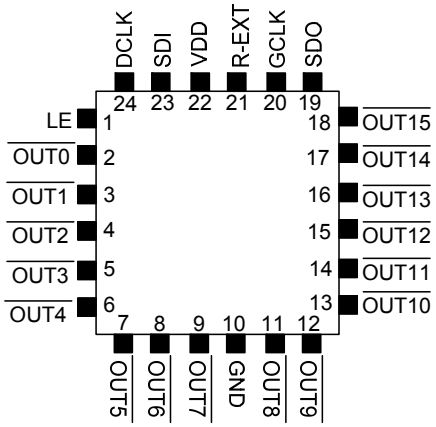


Figure 1

Pin Configuration



MBI5252 GP



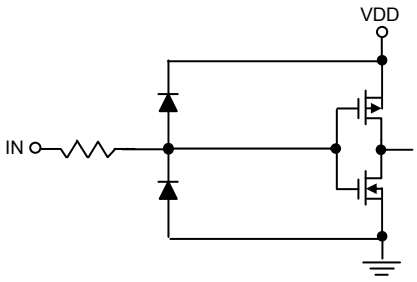
MBI5252 GFN

Terminal Description

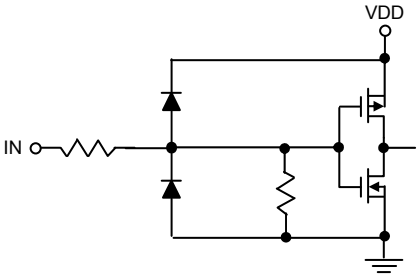
Pin Name	Function
GND	Ground terminal for control logic and current sink
SDI	Serial-data input to the shift register
DCLK	Clock input terminal used to shift data on rising edge and carries command information when LE is asserted.
LE	Data strobe terminal and controlling command with DCLK
$\overline{OUT0}$ ~ $\overline{OUT15}$	Constant current output terminals
GCLK	Gray scale clock terminal Clock input for gray scale. The gray scale display is counted by gray scale clock compared with input data.
SDO	Serial-data output to the receiver-end SDI of next LED driver
R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
VDD	3.3V/5V supply voltage terminal

Equivalent Circuits of Inputs and Outputs

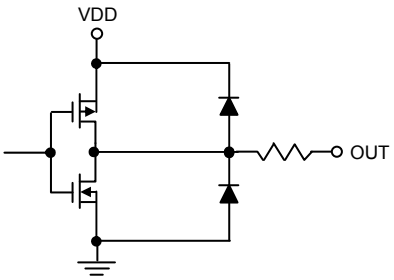
GCLK, DCLK, SDI terminal



LE Terminal



SDO Terminal



Maximum Rating

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0~7	V
Input Pin Voltage (SDI, DCLK, GCLK, LE)		V_{IN}	-0.4~V_{DD}+0.4	V
Sustaining Voltage at OUT Port		V_{DS}	-0.5~17	V
Output Current		I_{OUT}	+22	mA
GND Terminal Current		I_{GND}	360	mA
Power Dissipation (On 4 Layer PCB, Ta=25°C)*	GP Type	P_D	1.79	W
	GFN Type		3.12	
Thermal Resistance (On 4 Layer PCB, Ta=25°C)*	GP Type	$R_{th(j-a)}$	69.5	°C/W
	GFN Type		40.01	
Junction Temperature		$T_{j,max}$	150**	°C
Operating Ambient Temperature		T_{opr}	-40~+85	°C
Storage Temperature		T_{stg}	-55~+150	°C
ESD Rating	Human Body Mode (MIL-STD-883G Method 3015.7,)	HBM	Class 3B (8KV)	-
	Machine Mode (JEDEC EIA/ JESD22-A115,)	MM	Class C (400V)	-

*The PCB size is 76.2mm*114.3mm in simulation. Please refer to JEDEC JESD51.

** Operation at the maximum rating for extended periods may reduce the device reliability; therefore, the suggested junction temperature of the device is under 125°C.

Note: The performance of thermal dissipation is strongly related to the size of thermal pad, thickness and layer numbers of the PCB. The empirical thermal resistance may be different from simulative value. User should plan for expected thermal dissipation performance by selecting package and arranging layout of the PCB to maximize the capability.

Electrical Characteristics (V_{DD}=5.0V, Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		0.5	-	20	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	μA
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
		V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=1mA V_{DS}=1.0V	R_{ext}=14kΩ	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=1mA V_{DS}=1.0V	R_{ext}=14kΩ	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation*		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V, R_{ext}=1.4KΩ@10mA		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		$\%/dV_{DD}$	V_{DD} within 4.5V and 5.5V R_{ext}=1.4KΩ@10mA		-	±1.0	±2.0	% / V
LED Open Detection Threshold		$V_{OD,TH}$	-		-	0.5	-	V
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off" (SDI=DCLK =GCLK=0Hz)	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$~ $\overline{OUT15}$ =Off		-	4.5	5.5	mA
		I_{DD}(off) 3	R_{ext}=14KΩ, $\overline{OUT0}$~ $\overline{OUT15}$ =Off		-	5.0	6.0	
		I_{DD}(off) 4	R_{ext}=1.4KΩ, $\overline{OUT0}$~ $\overline{OUT15}$ =Off		-	6.5	8.0	
	"On" (SDI= DCLK=5MHz, GCLK=20MHz)	I_{DD}(on) 9	R_{ext}=14KΩ, $\overline{OUT0}$~ $\overline{OUT15}$ =On		-	6.5	8.0	
		I_{DD}(on) 10	R_{ext}=1.4KΩ, $\overline{OUT0}$~ $\overline{OUT15}$ =On		-	8.5	10	

*One channel on.

Electrical Characteristics (V_{DD}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Sustaining Voltage at OUT Ports		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT15}$		-	-	17	V
Output Current		I_{OUT}	Refer to "Test Circuit for Electrical Characteristics"		0.5	-	10	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta=-40~85ºC		0.7xV_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta=-40~85ºC		GND	-	0.3xV_{DD}	V
Output Leakage Current		I_{OH}	V_{DS}=17.0V		-	-	0.5	μA
Output Voltage	SDO	V_{OH}	I_{OH}=-1.0mA		V_{DD}-0.4	-	-	V
		V_{OL}	I_{OL}=+1.0mA		-	-	0.4	V
Current Skew (Channel)		dI_{OUT1}	I_{OUT}=1mA V_{DS}=1.0V	R_{ext}=14kΩ	-	±1.5	±2.5	%
Current Skew (IC)		dI_{OUT2}	I_{OUT}=1mA V_{DS}=1.0V	R_{ext}=14kΩ	-	±1.5	±3.0	%
Output Current vs. Output Voltage Regulation*		%/dV_{DS}	V_{DS} within 1.0V and 3.0V, R_{ext}=1.4KΩ@10mA		-	±0.1	±0.3	% / V
Output Current vs. Supply Voltage Regulation*		%/dV_{DD}	V_{DD} within 3.0V and 3.6V R_{ext}=1.4KΩ@10mA		-	±1.0	±2.0	% / V
LED Open Detection Threshold		$V_{OD,TH}$	-		-	0.3	-	V
Pull-down Resistor		R_{IN}(down)	LE		250	450	800	KΩ
Supply Current	"Off" (SDI=DCLK =GCLK=0Hz)	I_{DD}(off) 1	R_{ext}=Open, $\overline{OUT0}$~ $\overline{OUT15}$=Off		-	4.5	5	mA
		I_{DD}(off) 2	R_{ext}=14KΩ, $\overline{OUT0}$~ $\overline{OUT15}$=Off		-	4.5	5.5	
		I_{DD}(off) 3	R_{ext}=1.4KΩ, $\overline{OUT0}$~ $\overline{OUT15}$=Off		-	6.0	7.0	
	"On" (SDI= DCLK=5MHz, GCLK=20MHz)	I_{DD}(on) 2	R_{ext}=14KΩ, $\overline{OUT0}$~ $\overline{OUT15}$=On		-	6.0	7.0	
		I_{DD}(on) 3	R_{ext}=1.4KΩ, $\overline{OUT0}$~ $\overline{OUT15}$=On		-	7.5	9.0	

*One channel on.

Test Circuit for Electrical Characteristics

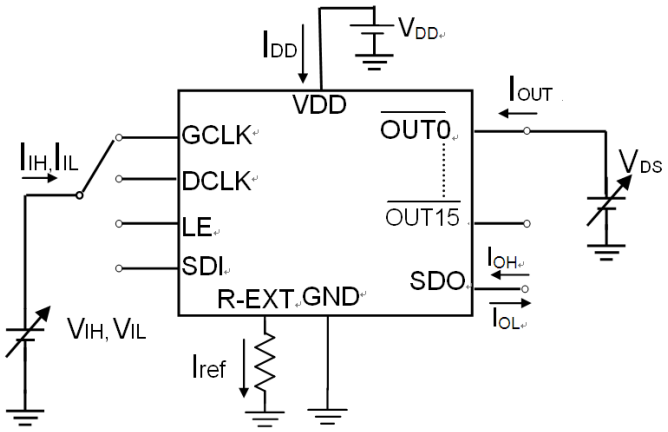


Figure 2

Switching Characteristics (V_{DD}=5.0V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}	V_{DD}=5.0V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=1.4KΩ V_{DS}=1V R_L=300Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4.0V	5	-	-	ns
	LE ↑ – DCLK ↑	t_{SU1}		8	-	-	ns
	LE ↓ (Vsync) – GCLK	t_{SU2}		1200			ns
	LE ↓ – DCLK ↑	t_{SU3}		50			ns
Hold Time	DCLK ↑ - SDI	t_{H0}		6	-	-	ns
	DCLK ↑ - LE	t_{H1}		8	-	-	ns
	GCLK – LE ↑ (Vsync)	t_{H2}		300			ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	22	25	ns
	GCLK – $\overline{OUT2n}$*	t_{PD1}		-	35	-	ns
	LE – SDO	t_{PD2}***		-	30	40	ns
Staggered Delay of Output	$\overline{OUT2n+1}$ **	t_{DL1}		-	5	-	ns
Pulse Width	LE	$t_{w(LE)}$		15			ns
Command to Command		Tcc		50	-	-	ns
Data Clock Frequency		F_{DCLK}		-	-	30	MHz
Gray Scale Clock Frequency***		F_{GCLK}		-	-	33	MHz
GCLK frequency (when GCLK multiplier is enabled)		F_{GCLK}				16.6	MHz
Min Clock(GCLK/DCLK) Pulse Width****		$t_{W(CLK)}$		12	-	-	ns
Ratio of (GCLK freq)/(DCLK freq)		$R_{(GCLK/DCLK)}$		20	-	-	%
Compulsory Error Detection Operation time*****		t_{ERR-C}		700	-	-	ns
Output Rise Time of Output Ports		t_{OR}		-	15	25	ns
Output Fall Time of Output Ports		t_{OF}		-	15	25	ns
Dead Time		t_{dth}		300			ns
Dead Time (Low state)		t_{dtl}		1200	-	-	ns

*Output waveforms have good uniformity among channels.

** Refer to the Timing Waveform, where n=0, 1, 2, 3, 4, 5, 6, 7.

***In timing of “configuration read”, the next DCLK rising edge should be t_{PD2} after LE’s falling edge.

****The Gray Scale Clock period must be 50% duty cycle when the function of GCLK multiplier is enabled.

*****Users have to leave more time than the maximum error detection time for the error detection.

Switching Characteristics (V_{DD}=3.3V, Ta=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Setup Time	SDI - DCLK ↑	t_{SU0}	V_{DD}=3.3V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=1.4KΩ V_{DS}=1V R_L=300Ω C_L=10pF C_1=100nF C_2=10μF C_{SDO}=10pF V_{LED}=4.0V	7	-	-	ns
	LE – DCLK ↑	t_{SU1}		10	-	-	ns
	LE ↓ (Vsync) – GCLK	t_{SU2}		1200	-	-	ns
	LE ↓ – DCLK ↑	t_{SU3}		52			ns
Hold Time	DCLK ↑ - SDI	t_{H0}		8	-	-	ns
	DCLK ↑ - LE	t_{H1}		10	-	-	ns
	GCLK – LE ↓ (Vsync)	t_{H2}		300	-	-	ns
Propagation Delay Time	DCLK – SDO	t_{PD0}		-	25	30	ns
	GCLK –$\overline{OUT2n}$*	t_{PD1}		-	45	-	ns
	LE – SDO	t_{PD2}***			40	50	ns
Staggered Delay of Output	$\overline{OUT2n+1}$ **	t_{DL1}		-	8	-	ns
Pulse Width	LE	$t_{w(LE)}$		16			ns
Command to Command		tcc		52	-	-	ns
Data Clock Frequency		F_{DCLK}		-	-	25	MHz
Gray Scale Clock Frequency****		F_{GCLK}		-	-	20	MHz
GCLK frequency (when GCLK multiplier is enabled)		F_{GCLK}				10	MHz
Min Clock(GCLK/DCLK) Pulse Width****		$t_{W(CLK)}$		13			ns
Ratio of (GCLK freq)/(DCLK freq)		$R_{(GCLK/DCLK)}$		20		-	%
Compulsory Error Detection Operation time*****		t_{ERR-C}		700	-	-	ns
Output Rise Time of Output Ports		t_{OR}			25	35	ns
Output Fall Time of Output Ports		t_{OF}			25	35	ns
Dead Time		tdth		300	-	-	ns
Dead Time (Low state)		tdtl		1200	-	-	ns

*Output waveforms have good uniformity among channels.

** Refer to the Timing Waveform, where n=0, 1, 2, 3, 4, 5, 6, 7.

***In timing of “configuration read”, the next DCLK rising edge should be t_{PD2} after LE’s falling edge.

****The Gray Scale Clock period must be 50% duty cycle when the function of GCLK multiplier is enabled.

*****Users have to leave more time than the maximum error detection time for the error detection.

Test Circuit for Switching Characteristics

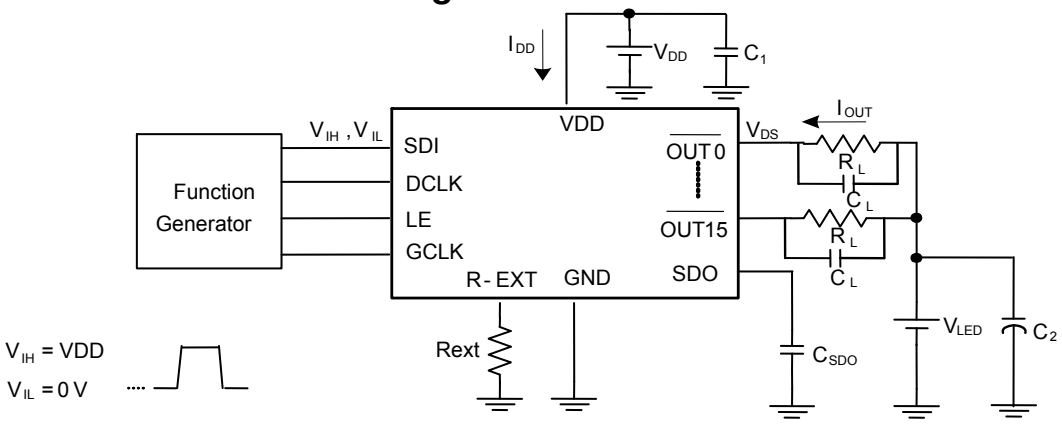
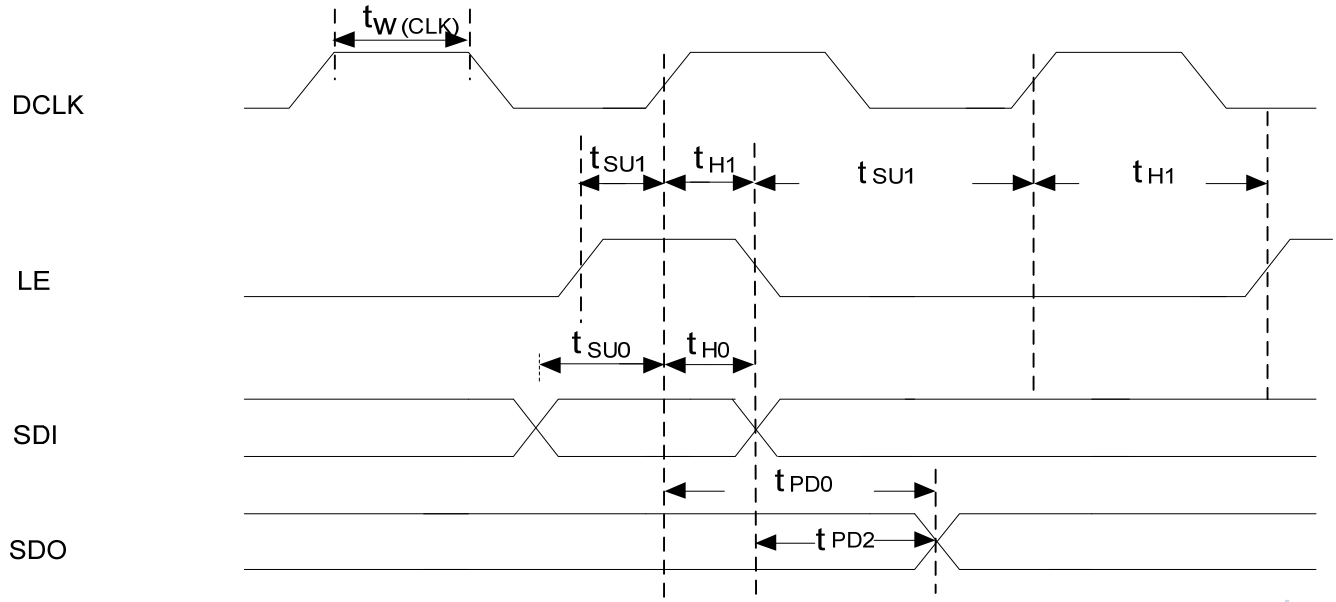
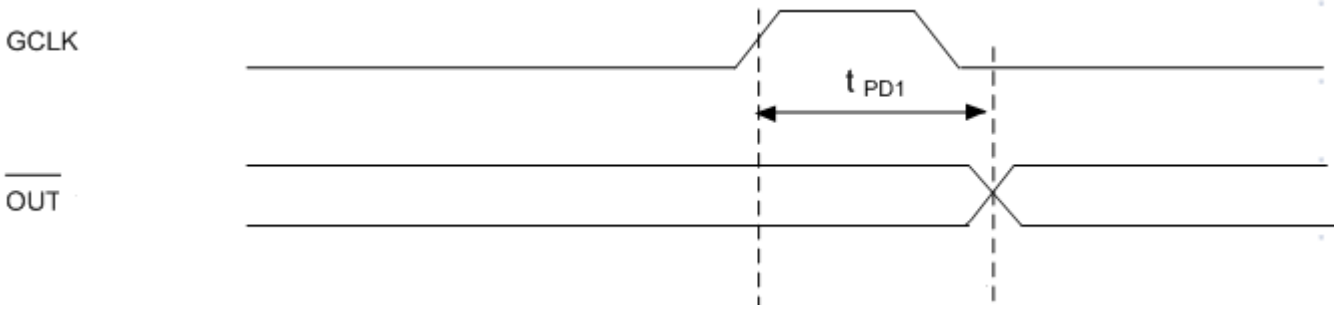
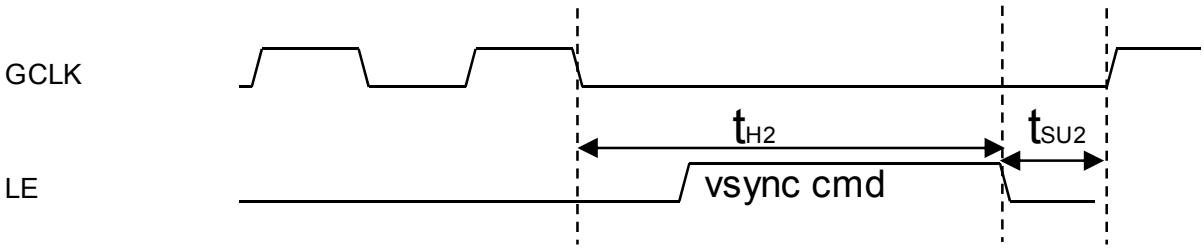


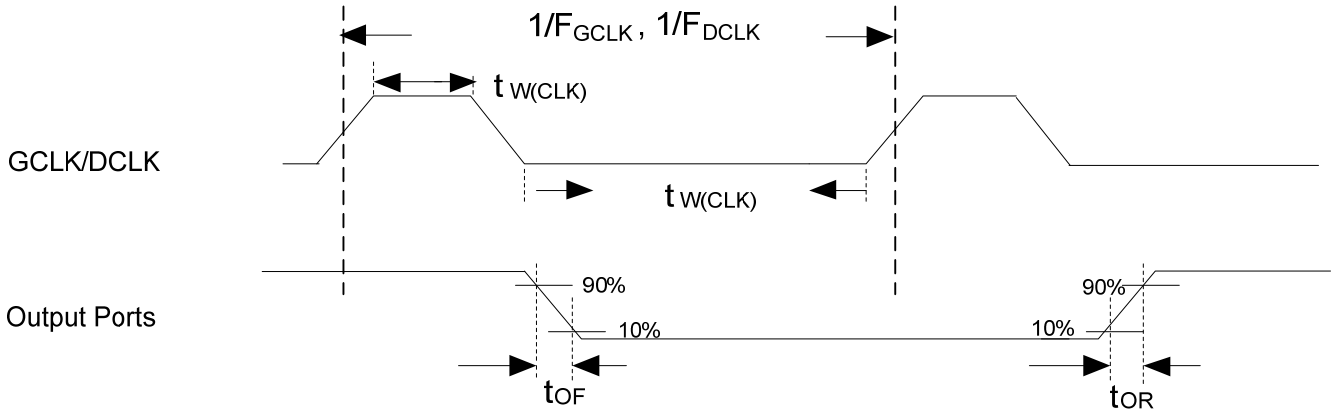
Figure 3

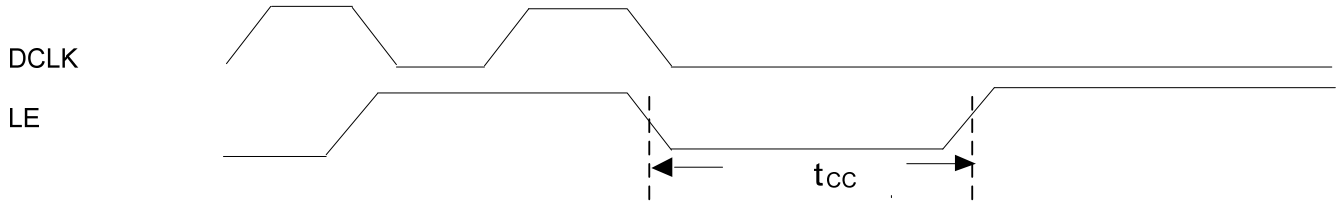
Timing Waveform

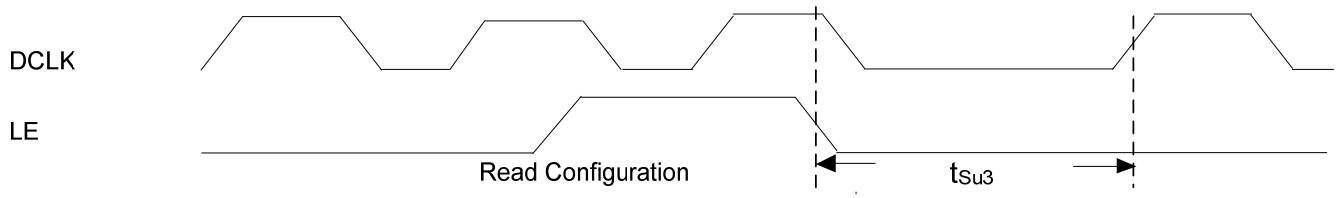


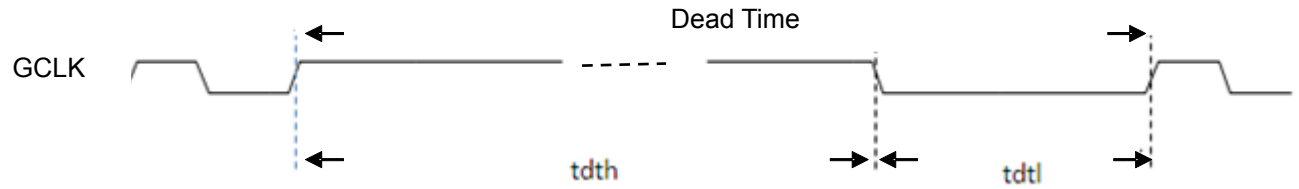





1/F GCLK , 1/F DCLK
t W(CLK)
GCLK/DCLK
t W(CLK)
Output Ports
90%
10%
90%
10%
tOF
tOR


DCLK
LE
tCC


DCLK
LE
Read Configuration
tSu3


Dead Time
GCLK
tdth
tdtl

Control Command

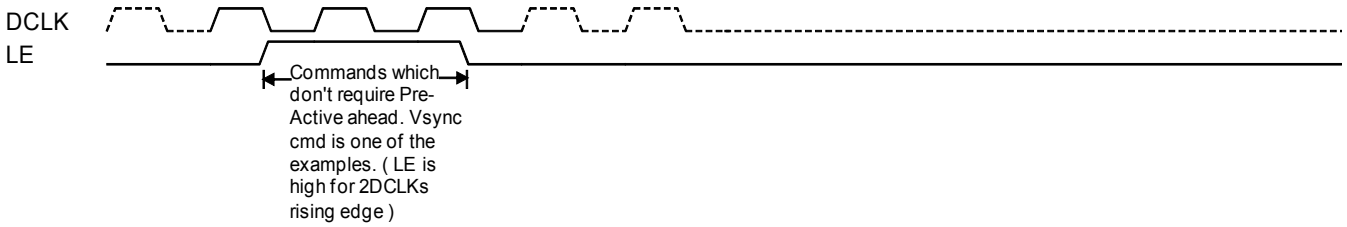
Command Name	Signals Combination		Description
	LE	Number of DCLK Rising Edge when LE is asserted	Action of Command
Stop Compulsory Error detection	High	1	Stop compulsory LED open detection.
Data Latch	High	1	Serial data are transferred to the input data buffers.
VSYNC	High	2	Vertical Synchronal signal. Displaying frame will be updated to output channel.
Write Configuration 1*	High	4	Serial data are written to the configuration register.1
Read Configuration 1	High	5	Serial data are read from the configuration register.1
Start Compulsory Error detection	High	7	Start compulsory LED open detection
Write Configuration 2*	High	8	Serial data are written to the configuration register.2
Read Configuration 2	High	9	Serial data are read from the configuration register.2
Software Reset	High	10	Reset the behavior of MBI5252 except the value of configuration registers.
Pre-Active	High	14	Pre-Active command needs to be sent before “Write Configuration” command.

*Those commands can only be activated after Pre-Active command; otherwise, they will be invalid.

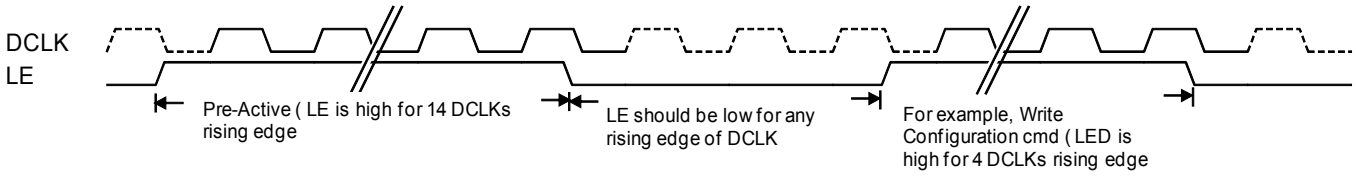
Note: When the power is on, Vsync command will be valid only after 16 times of “Data Latch” commands that have been sent in advance.

The following figures show the waveforms of commands which require or don’t require “Pre-Active” ahead.

Commands which don't require Pre-Active ahead



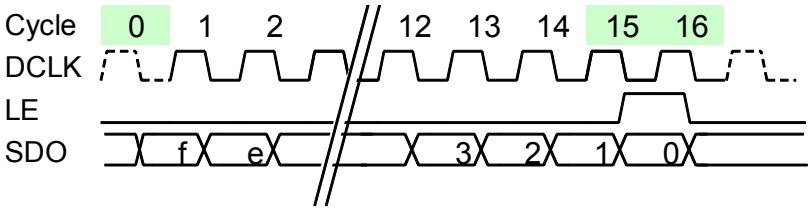
Commands which require Pre-Active ahead



Waveform of Commands

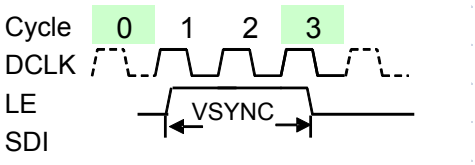
The following figures show the waveforms of each command.

Data Latch



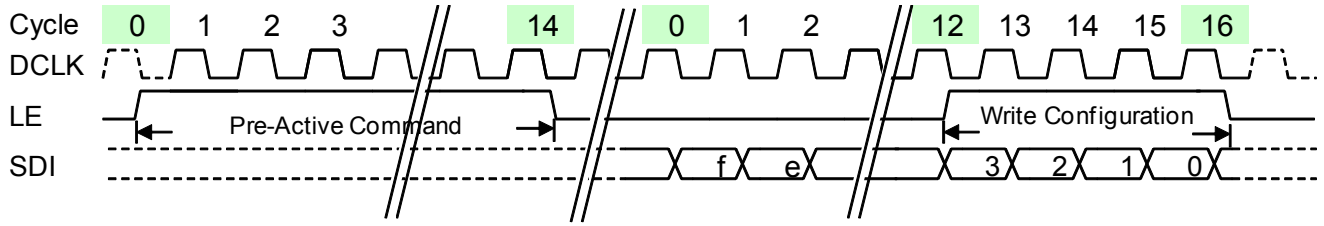
Data Latch command is used to latch the 16-bit shift register from SDI to internal SRAM buffer. When this command is received, the last 16 bits data before the falling edge of LE will be latched into SRAM, as shown in the above waveform, and MSB bit needs to be sent first.

Vertical Sync (VSYNC)



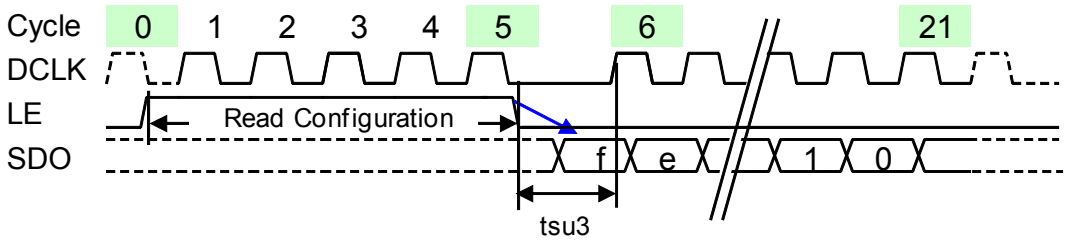
"VSYNC" command is used to update frame data on output channels ($\overline{OUT0}$~ $\overline{OUT15}$). There are some timing limitations between signal "LE" and "GCLK"; and please refer to the section of "Vsync Command Operation" for details.

Write Configuration



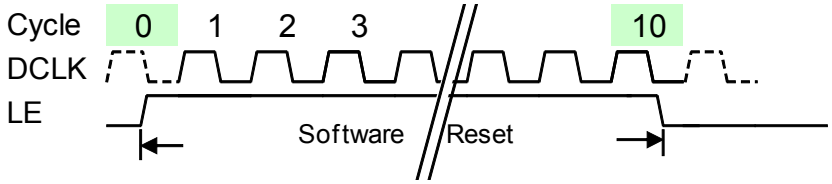
"Write configuration" command is used to program the configuration register of MBI5252. The "Pre-Active" command must be sent in advance. When this command is received, the last 16 bits data before the falling edge of LE will be latched into configuration register, as shown in the above waveform, and MSB bit needs to be sent first.

Read Configuration



"Read configuration" command is used to read the configuration register of MBI5252. When this command is received, the 16-bit data of configuration register will be shifted out from SDO pin, as shown in the above waveform, and MSB bit will be shifted out first.

Software Reset



"Software reset" command makes MBI5252 go back to the initial state except configuration register value. After this command is received, the output channels will be turned off and will display again with last gray-scale value after new "Vsync" command is received.

Definition of Configuration Register 1

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	101011					

Default setting of configuration register is 16'h032B

Bit	Attribute	Definition	Value	Function
F	Read/Write	Lower ghost elimination	0 (Default)	0:Disable
				1:Enabled
E~C	Reserved	Reserved	000 (Default)	Reserved
B-8	Read/Write	Number of scan lines	0000 0001 0010 0011 (**Default**) ~ 1111	0000: 1 line 0001: 2 lines 0010: 3 lines 0011: 4 lines …….. 1110: 15 lines 1111: 16 lines
7	Read/Write	Gray scale mode	0 (Default)	The 16384 GCLKs (14-bit) PWM cycle is divided into 32 sections, and each section has 512 GCLKs.
			1	The 8192 GCLKs(13-bit) PWM cycle is divided into 16 sections, and each section has 512 GCLKs.,
6	Read/Write	GCLK multiplier	0 (Default)	GCLK multiplier disable
			1	GCLK multiplier enable
5~0	Read/Write	Current gain adjustment	000000~111111	6'b101011 (Default) Allow 64-step programmable current gain from 12.5 % to 200%

Definition of Configuration Register 2

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Default setting of configuration register is 16'h032B

Bit	Attribute	Definition	Value	Function
F~B	Reserved	Reserved	Reserved	Reserved
A	Read/Write	Double refresh rate	0(Default)	0: Disable 1: Enable
9~4	Reserved	Reserved	Reserved	Reserved
3~1	Read/Write	dim line compensation	000 (Default)	000: 0 ns, 100: 20ns 001: 5 ns, 101: 25ns 010: 10 ns, 110: 30ns 011: 15 ns, 111: 35ns
0	Reserved	Reserved	Reserved	Reserved

Number of Scan Line

MBI5252 supports 1 to 16 scan lines. Please set the configuration register1 bit [B:8] according to the application. The default value '0011' is 4 scan lines.

Gray Scale Mode and Scan-type S-PWM

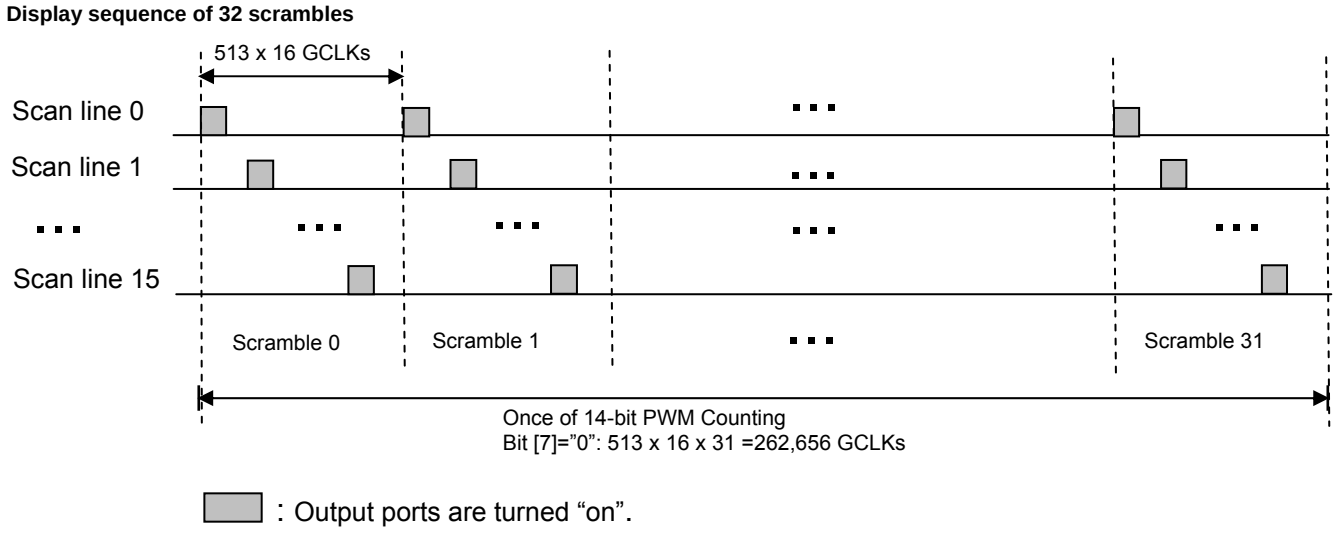
MBI5252 provides a selectable 14-bit or 13-bit gray scale by setting the configuration register1 bit [7]. The default value is set to '0' for 14-bit color depth. In 14-bit gray scale mode, users should still send 16-bit data with 2-bit '0' in LSB bits. For example, {14'h1234, 2'h0}.

MBI5252 has a smart S-PWM technology for scan type. With S-PWM, the total PWM cycles can be broken into MSB (Most Significant Bits) and LSB (Least Significant Bits) of gray scale cycles. The MSB information can be broken down into many refresh cycles to achieve overall same high bit resolution.

GCLK multiplier

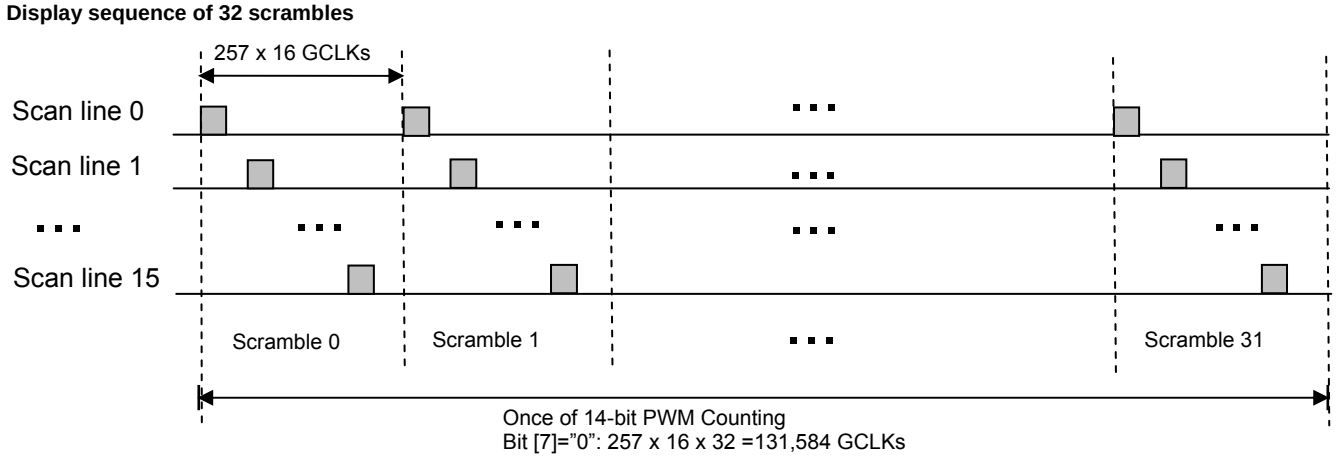
MBI5252 provides a GCLK multiplier function by setting the configuration register1 bit [6]. The default value is set to '0' for GCLK multiplier disable.

GCLK multiplier disabled (configuration register1 bit [6] = 0)



: Output ports are turned "on".

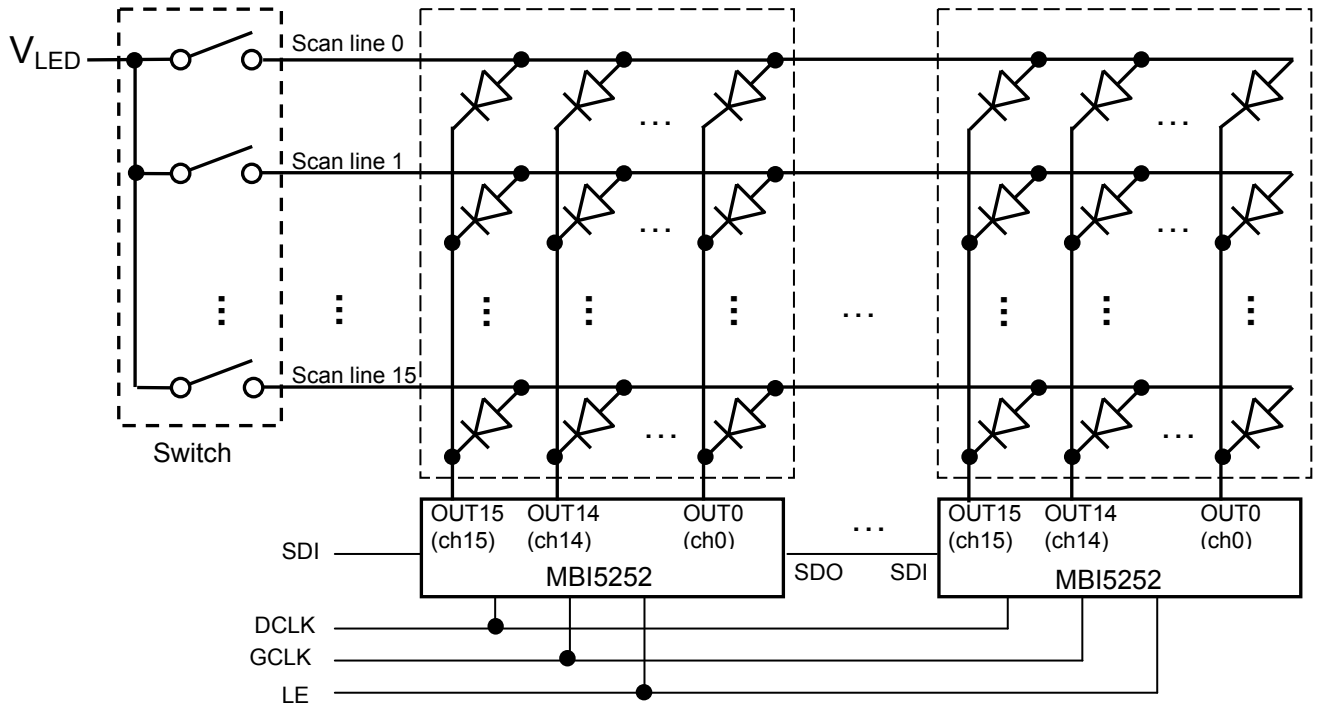
GCLK multiplier enabled (configuration register1 bit [6] = 1)



: Output ports are turned "on".

Operation Principal

Scan type application structure



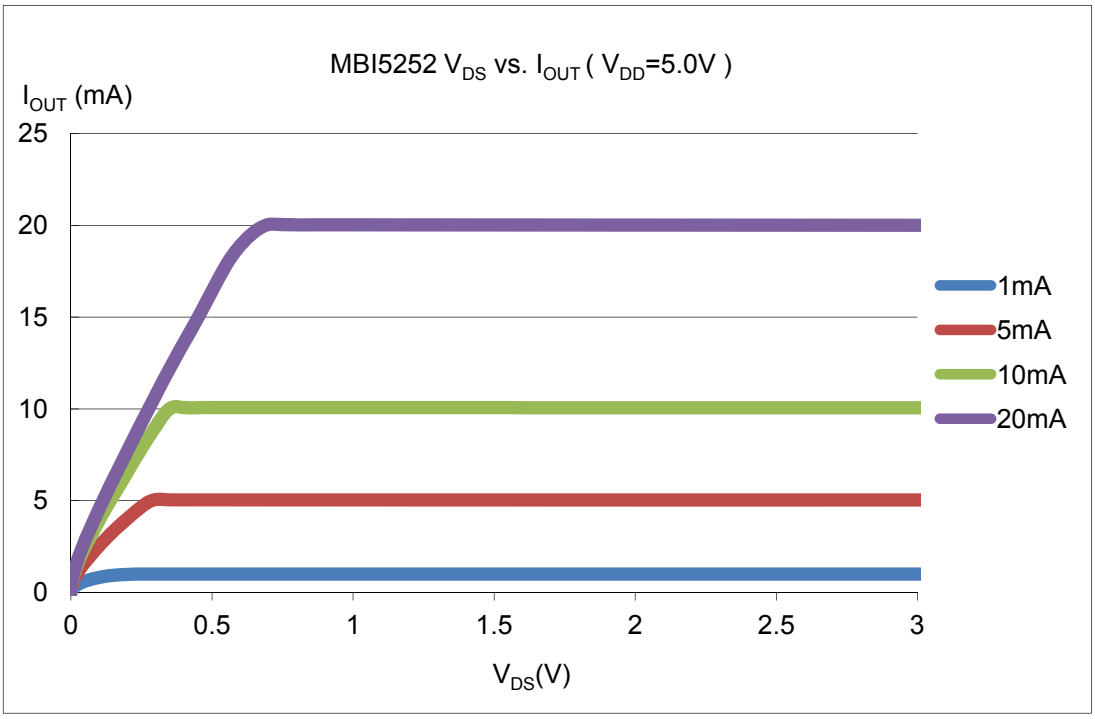
The above figure shows the suggested application structure of scan type scheme with 16 scan lines. The gray-scale data are sent by pin “SDI and SDO” with the commands formed by pin “LE” and “DCLK”. The output ports from 16 channels ($\overline{OUT0}$~ $\overline{OUT15}$) will output the PWM result for each scan line at different time, so there must be one “Switch” to multiplex for each scan line. The switching sequence and method and the command usage will be described in the application note.

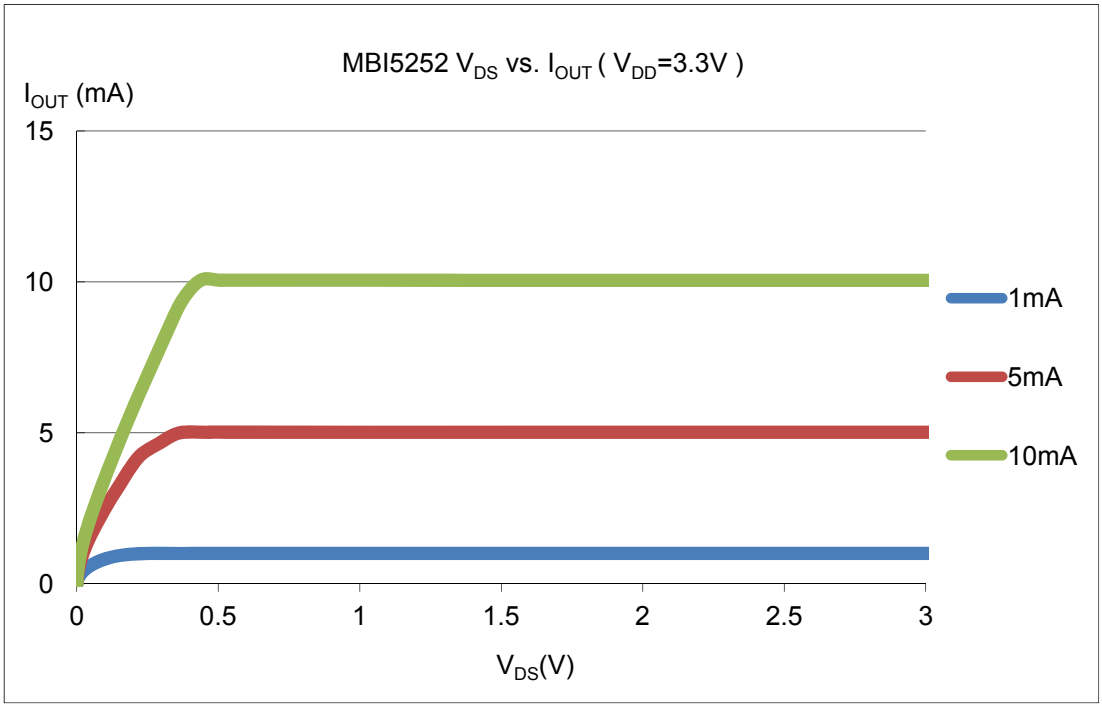
Constant Current

In LED display application, MBI5252 provides nearly no variation in current from channel to channel and from IC to IC. This can be achieved by:

1) The maximuml current variation between channels is less than 2.5%, and that between ICs is less than ±3%

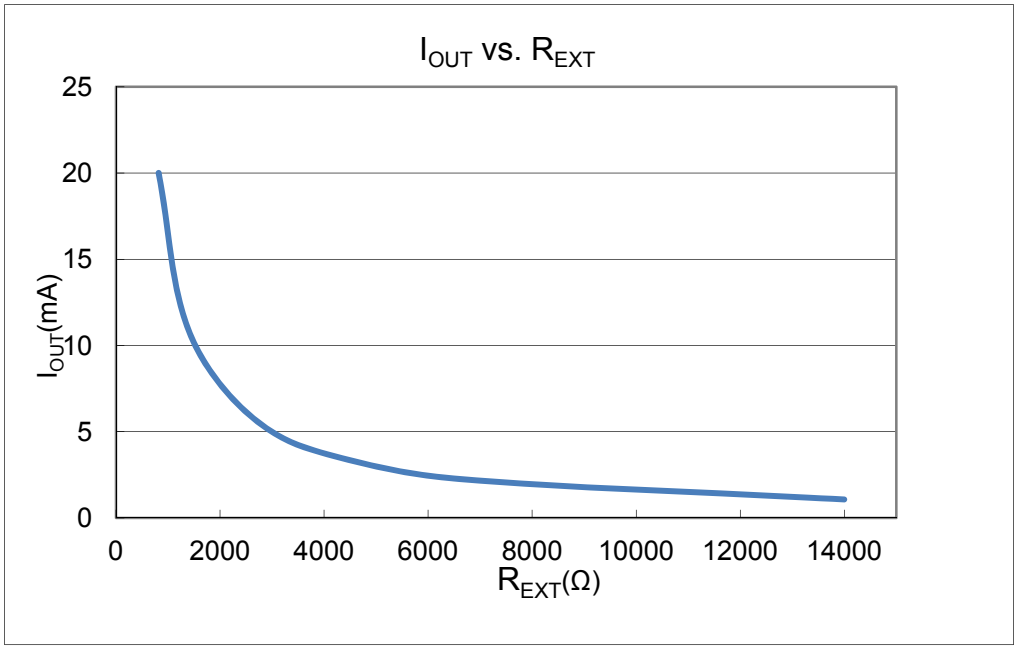
2) In addition, the current characteristic of output stage is flat and user can refer to the figure below. The output current can be kept constant regardless of the variations of LED forward voltages (V_F). This guarantees LED to be performed on the same brightness as user's specification.





Setting Output Current

The output current (I_{OUT}) is set by an external resistor, R_{ext}. The default relationship between I_{OUT} and R_{ext} is shown in the following figure.

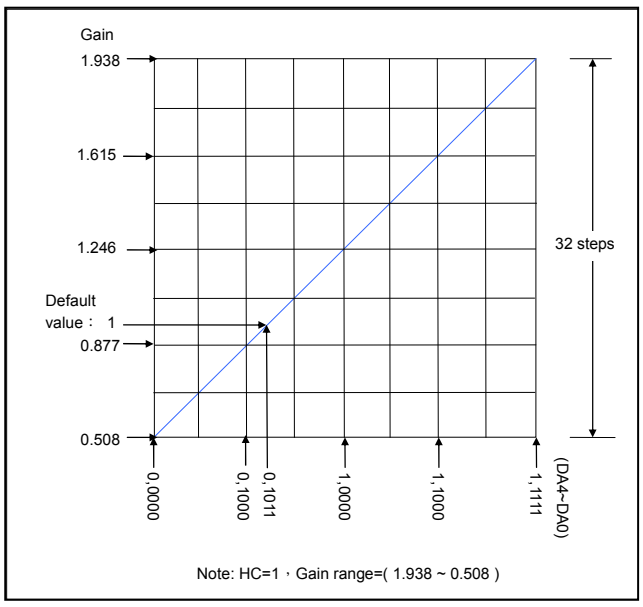


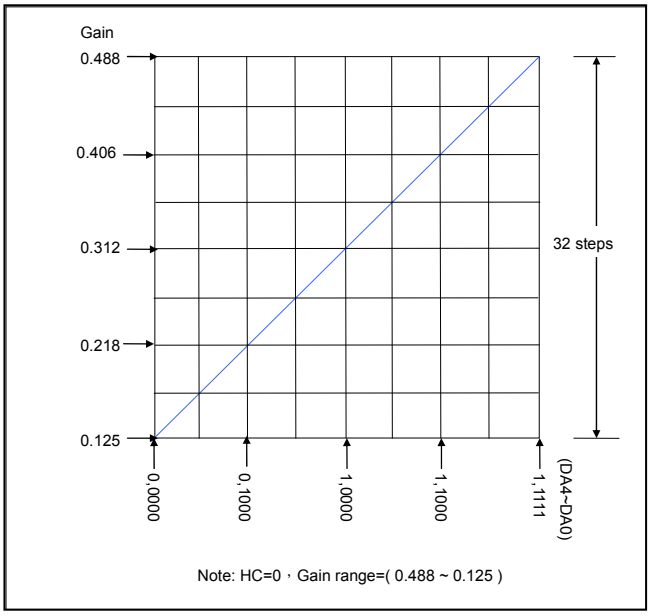
Also, the output current can be calculated from the equation:

$V_{R\text{-}EXT}$=0.61Volt x G; I_{OUT}= ($V_{R\text{-}EXT}/R_{ext}$) x24.0

Whereas R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is its voltage. G is the digital current gain, which is set by the bit5 – bit0 of the configuration register. The default value of G is 1. The formula and setting for G are described in next section.

Current Gain Adjustment





The 6 bits (bit 5~bit 0) of the configuration register set the gain of output current, i.e., G. As total 6-bit in number, i.e., ranging from 6'b000000 to 6'b111111, these bits allow user to set the output current gain up to 64 levels. These bits can be further defined inside configuration register as follows:

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	HC	DA4	DA3	DA2	DA1	DA0

1. Bit 5 is HC bit. The setting is in low current band when HC=0, and in high current band when HC=1.
2. Bit 4 to bit 0 are DA4 ~ DA0.

The relationship between these bits and current gain G is:

HC=1, D=(65xG-33)/3

HC=0, D=(256xG-32)/3

and D in the above decimal numeration can be converted to its equivalent in binary form by the following equation:

$D= DA4x2^4+DA3x2^3+DA2x2^2+DA1x2^1+DA0x2^0$

In other words, these bits can be looked as a floating number with 1-bit exponent HC and 5-bit mantissa DA4~DA0.

For example,

HC=1, G=1.246, D=(65x1.246-33)/3=16

the D in binary form would be:

$D=16=1x2^4+0x2^3+0x2^2+0x2^1+0x2^0$

The 6 bits (bit 5~bit 0) of the configuration register are set to 6'b110000.

Package Power Dissipation (PD)

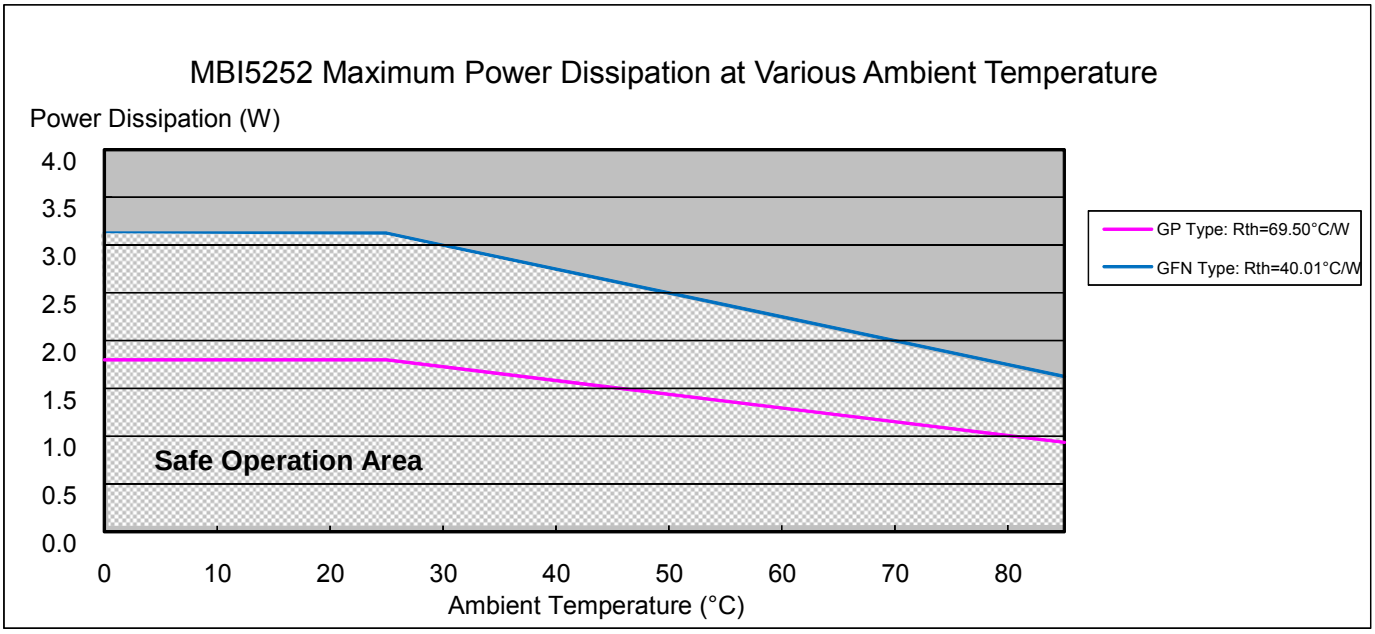
The maximum allowable package power dissipation is determined as $P_D(max)=(Tj–Ta)/R_{th(j-a)}$. When 16 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act)=(I_{DD}xV_{DD})+(I_{OUT}xDutyxV_{DS}x16)$. Therefore, to keep $P_D(act)\leq P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT}=\{[(Tj–Ta)/R_{th(j-a)}]–(I_{DD}xV_{DD})\}/V_{DS}/Duty/16$, where Tj=150°C.

Please see the follow table for P_D and $R_{th(j-a)}$ for different packages:

Device Type	$R_{th(j-a)}$ (°C/W)	P_D (W)
GP	69.50	1.79
GFN	40.01	3.12

The maximum power dissipation, $P_D(max)=(Tj–Ta)/R_{th(j-a)}$, decreases as the ambient temperature increases.



LED Supply Voltage (V_{LED})

MBI5252 is designed to operate with V_{DS} ranging from 0.4V to 1.0V (depending on I_{OUT}=0.5~20mA) considering the package power dissipating limits. V_{DS} may be higher enough to make $P_{D\ (act)} > P_{D\ (max)}$ when V_{LED}=5V and $V_{DS}=V_{LED}-V_F$, in which V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets $V_{DS}=(V_{LED}-V_F)-V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.

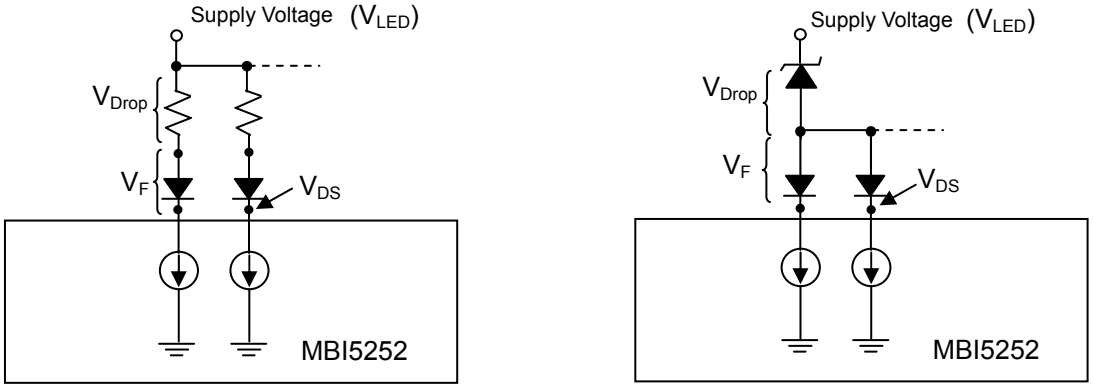


Figure 5

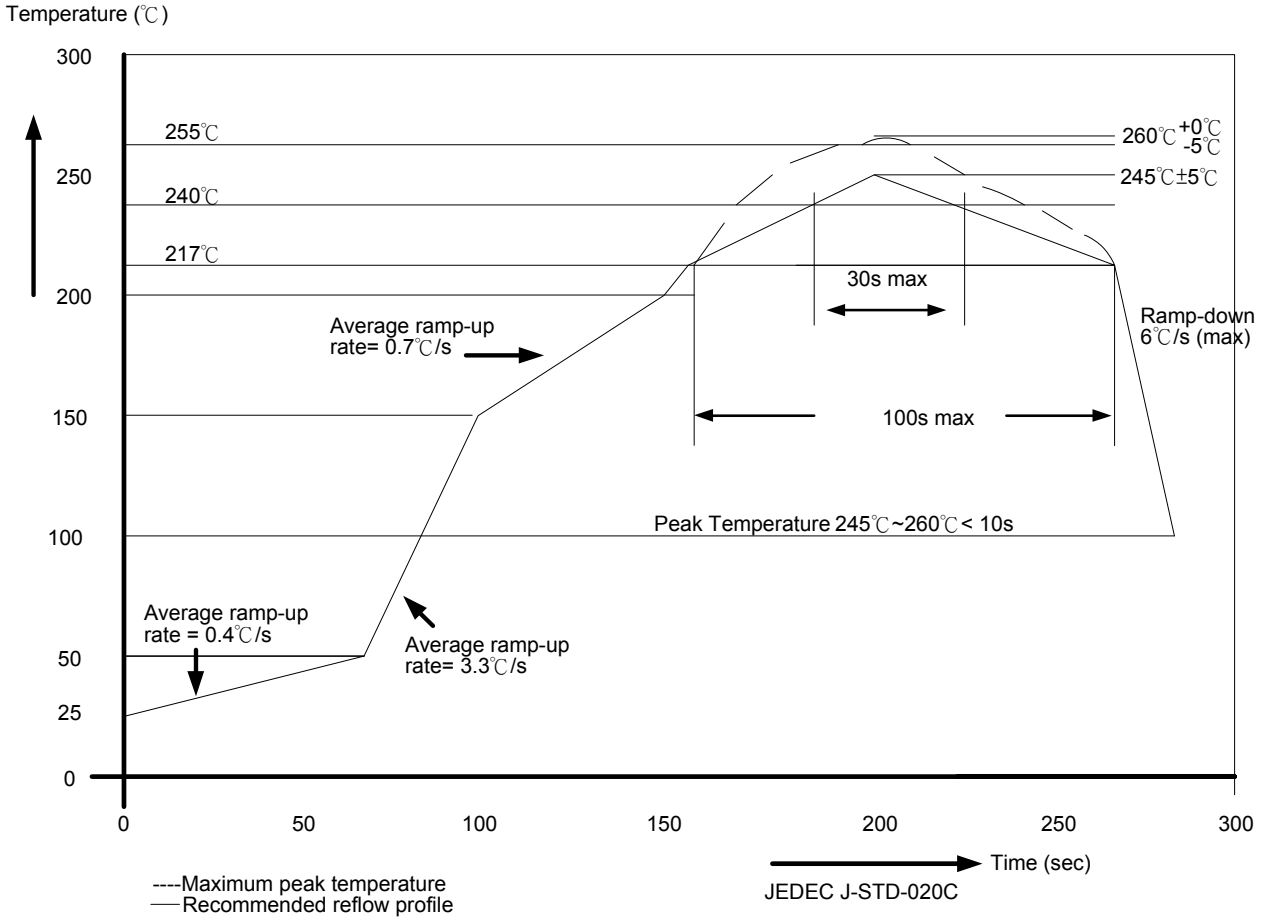
Switching Noise Reduction

LED drivers are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers- Overshoot”.

Soldering Process of "Pb-free & Green" Package Plating*

Macroblock has defined "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected 100% pure tin (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it adopts tin/lead (SnPb) solder paste, and please refer to the JEDEC J-STD-020C for the temperature of solder bath. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn) will all require from 245 °C to 260°C for proper soldering on boards, referring to JEDEC J-STD-020C as shown below.

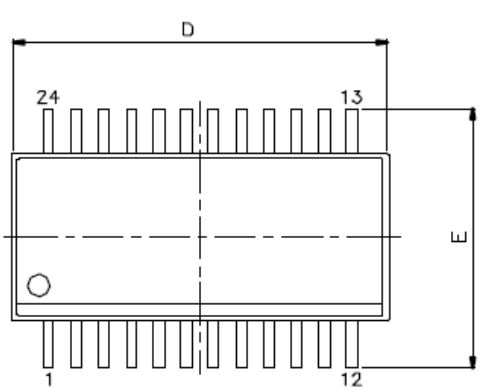
For managing MSL3 Package, it should refer to JEDEC J-STD-020C about floor life management & refer to JEDEC J-STD-033C about re-bake condition while IC's floor life exceeds MSL3 limitation.

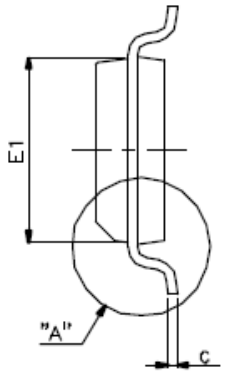


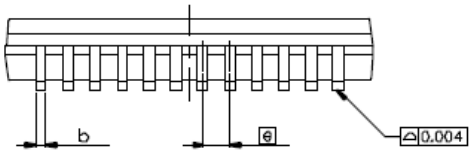
Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 ≧2000
<1.6mm	260 +0 °C	260 +0 °C	260 +0 °C
1.6mm – 2.5mm	260 +0 °C	250 +0 °C	245 +0 °C
≧2.5mm	250 +0 °C	245 +0 °C	245 +0 °C

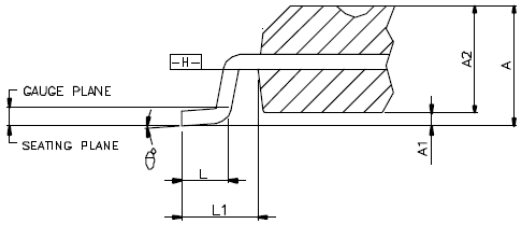
*For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Outline



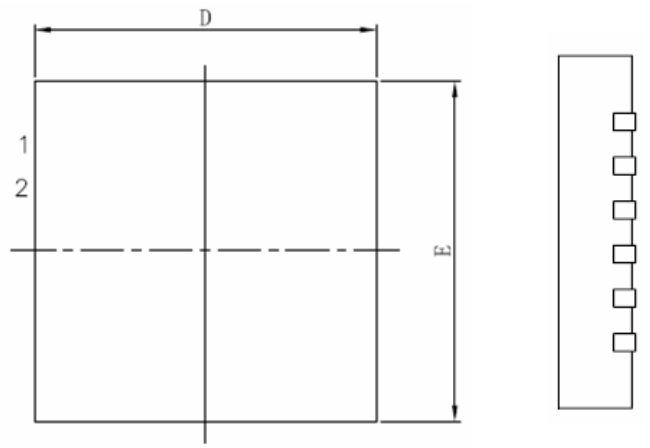


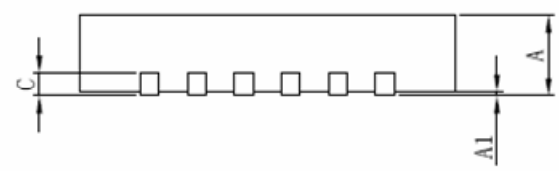


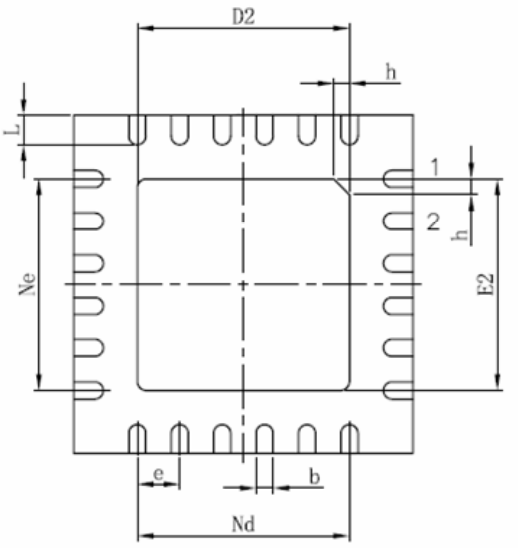


SYMBOLS	Dimensions shown in inchs			Dimensions shown in millimeters		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.053	0.064	0.069	1.346	1.626	1.753
A1	0.004	0.006	0.010	0.102	0.152	0.254
A2	—	—	0.059	—	—	1.499
D	0.337	0.341	0.344	8.560	8.661	8.738
E	0.228	0.236	0.244	5.791	5.994	6.198
E1	0.150	0.154	0.157	3.810	3.912	3.988
b	0.008	—	0.012	0.203	—	0.305
c	0.007	—	0.010	0.178	—	0.254
L	0.016	0.025	0.050	0.406	0.635	1.270
e	0.025 BASIC			0.635 BASIC		
L1	0.041 BASIC			1.0414 BASIC		
Θ°	0	—	8	0	—	8

MBI5252 GP Outline Drawing





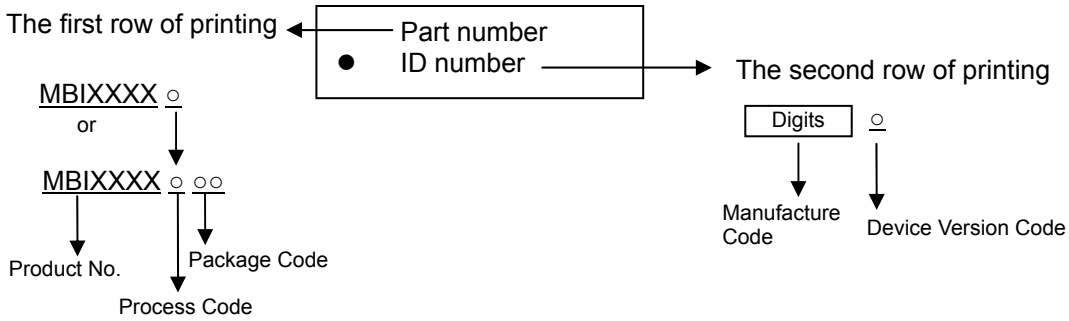


SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	—	0.01	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.50REF		
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.50REF		
L	0.35	0.40	0.45
h	0.30	0.35	0.40

MBI5252 GFN Outline Drawing

Note 1: The unit of the outline drawing is millimeter (mm).
Note 2: The thermal pad size may exist a tolerance due to the manufacturing process, please use the maximum dimensions-D2 (max. 2.50mm) x E2 (max. 2.50mm) for the thermal pad layout. In addition, to avoid the short circuit risk, the circuit traces shall not pass through the maximum area of thermal pad.

Product Top Mark Information



Product Revision History

Datasheet Version	Devise Version Code
V1.00	A

Product Ordering Information

Product Ordering Number*	RoHS Compliant Package Type	Weight (g)
MBI5252GP-A	SSOP24L-150-0.64	0.11
MBI5252GFN-A	QFN24L-4*4-0.5	0.0379

*Please place your order with the ***"product ordering number"*** information on your purchase order (PO).

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